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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,907	08/15/2000	Thomas M. Olano	15-4-897.00	1122

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EXAMINER
NGUYEN, HAU H

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/638,907	Applicant(s) OLANO ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-8, 11-18, 21-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Grossman et al. (U.S. Patent No. 5,230,039).

Referring to claims 1-2, 11-12, 21-23, Grossman et al. teach a means and a method for specifying and controlling a display range in which a specified form of texture mapping is applied or suppressed. Object data from a host computer is processed by four pipelined graphics subsystems before being displayed on a display screen. These graphics subsystems include: 1) a Geometry Subsystem, 2) a Scan Conversion Subsystem, 3) a Raster Subsystem, and 4) a Display Subsystem, wherein the Raster Subsystem also performs various blending and texturing functions on a pixel-by-pixel basis as the pixels are written to image bit-planes, or a frame buffer (col. 2, lines 5-22). The Display Subsystem receives pixel information from the frame buffer, routes it through the appropriate display mode, and sends it to the Digital-to-Analog Converters for display. Five Multimode Graphics Processors (MGPs) read and interpret the contents of the Image Planes (col. 6, lines 61-66). One of the major components of the Geometry Subsystem is the single-instruction, multiple-data (SIMD)-organized Geometry Engine (col. 4, lines 2-5). The Geometry Engine (GE) processes a stream of high-level graphics commands mixed with single-precision, floating point data. Each GE module includes local memory data. The four modules

act together as a SIMD machine under control of a centralized micro-sequencer, operating on up to four graphic object vertices simultaneously (col. 4, lines 32-38). The first Geometry Engine task is to perform matrix operations on incoming vertices. Each Geometry Engine uses a 4 X 4 matrix stack to rotate, translate, and scale 2D and 3D homogeneous coordinates (col. 4, lines 41-46). With reference to Fig. 3, the field definitions within an input texture map coordinate 301 are illustrated. Such a texture map coordinate 301 is used to define s or t positions within a texture map. One coordinate is associated with the s direction; another coordinate is associated with the t direction. Several fields are provided within each texture coordinate 301. The coordinate fraction field 303 defines a location associated with a particular texel with a texture map. Field 305 represents actual texture map address bits. Field 304 represents fractional address bits; it is used to blend the value of texels at adjacent addresses (col. 9, lines 10-27). The retrieval of the above-described input coordinates is performed by the span processor 120 as shown in Figs. 5a and 5b (and col. 10, lines 61-66). FIG. 6 is an example of manipulating a texture space comprising multiple sets of texture maps (col. 12, lines 13-17).

In regard to claims 3-4, 13-14, as cited above, Grossman et al. teach the data is read out from frame buffer, which copies and stores the set of data (see col. 3, lines 56-62).

Referring to claims 5-6, 15-16, as cited above, Grossman et al. teach the field definitions within an input texture map coordinate 301 are illustrated in Fig. 3. Such a texture map coordinate 301 is used to define s or t positions within a texture map. One coordinate is associated with the s direction; another coordinate is associated with the t direction (col. 9, lines 10-27).

In regard to claims 7 and 17, as cited above with reference to Figs. 5a and 5b, Grossman teach the span processor 120 microcode controls the activation of the logic illustrated in FIGS. 5a and 5b. Once activated, this processing logic begins execution starting at a bubble labeled start 501 illustrated in FIG. 5a. The input coordinate, of a form similar to that described in relation to FIG. 3a, is retrieved (col. 10, lines 61-66).

In regard to claims 8 and 18, Grossman et al. teach the Raster Subsystem also performs various blending and texturing functions on a pixel-by-pixel basis as the pixels are written to image bit-planes, or a frame buffer (col. 2, lines 19-22).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-10, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grossman et al. (U.S. Patent No. 5,230,039) in view of Krech, Jr. (U.S. Patent No. (6,057,852). Referring to claims 9 and 10, as applied to claim 2 above, Grossman et al. teach all the limitations of claims 9 and 10, except for software used to support the method is graphics application interface (API), and the graphics API is OpenGL with texture extension.

However, as cited by Krech, OpenGL is a widely used graphics API, which is rapidly becoming an industry standard since it does not require such a color command to be associated with the drawing instruction/command (col. 2, lines 60-63).

Therefore, it would have been obvious to one skilled in the art to utilize OpenGL API as described by Krech in combination with the method for perform SIMD instructions as taught by Grossman et al. because OpenGL offers a robust, yet flexible, programming interface, and does not require a programmer to include a color command with each graphic primitive (col. 2, lines 64-66).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

Agarwal et al. (US Patent No. 5,513,366) teach a method for executing SIMD instructions with the steps of storing/reading/retrieving as shown in Fig. 6.

Poulton et al. (US Patent No. 5481669) disclose an image generation and memory architecture having a SIMD rasterizer with a local external memory for storing texture information.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

01/20/2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600